REMARKS

The rejections and comments of the Examiner set forth in the Office Action dated August 16, 2000 have been carefully reviewed by the Applicants. In response, Applicants have amended the claims. Applicants respectfully request the Examiner to consider and allow the amended claims.

Claims 11-3, 5-10, 12-14, and 18-20 stand rejected under 35 U.S.C. §103(a) as being anticipated by Hathaway et al. (U.S. Patent No. 5,757,657) in view of Shouen (U.S. Patent No. 6,086,625). The Hathaway reference pertains to an adaptive incremental placement process of circuits on a VLSI chip. More specifically, Hathaway relates to a computer implemented method that incrementally updates a design placement in a VLSI chip. The Shouen patent pertains to a method and apparatus for designing a circuit by describing logic design information with a hardware description language.

In response, Applicants have amended independent Claims 1, 10, and 18 to include the limitations wherein the physical placement of an integrated circuit is adaptive to changes made to the netlist during the rough placement process until convergence is achieved. Convergence is achieved during rough placement by "b) executing a cell separation process according to the netlist, wherein cells are placed at locations; c) changing the netlist; d) modifying spacings of the cells responsive to changes made to the netlist, wherein a placement of the cells are changed according to the changes made to the netlist; e) partitioning the cells into a plurality of partitions; f) changing the placement of the cells after a partition is created."

The significance of the present invention is that by allowing netlist changes to be entered during the rough placement process, the overall number of iterations required for the design of the integrated circuits is minimized. Applicants respectfully submit that neither Hathaway, Shouen, either separately or combined teach, disclose, suggest, or render obvious the present invention of adaptively changing the physical placement of an integrated circuit is as a function of changes made to the netlist during the rough placement process until convergence is achieved and then performing a detailed place and route process.

Therefore, it is respectfully submitted that all claims are now in condition for allowance and such action is earnestly solicited by the Applicants.

If there are any additional charges, please charge them to our Deposit Account Number 23-0085.

Respectfully submitted,

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Date: 1/9, 2001

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